

FEATURES

Eight Single Ended Line Drivers in One Package
Meets EIA Standard RS-232E, RS-423A and
CCITT V.10/X.26

Resistor Programmable Slew Rate

Wide Supply Voltage Range

Low Power CMOS

3-State Outputs

TTL/CMOS Compatible Inputs

Output Short Circuit Protection

Available in 28-Pin DIP/PLCC

Low Power Replacement for UC5170C

APPLICATIONS

High Speed Communication

Computer I-O Ports Peripherals

High Speed Modems

Printers

Logic Level Translation

GENERAL DESCRIPTION

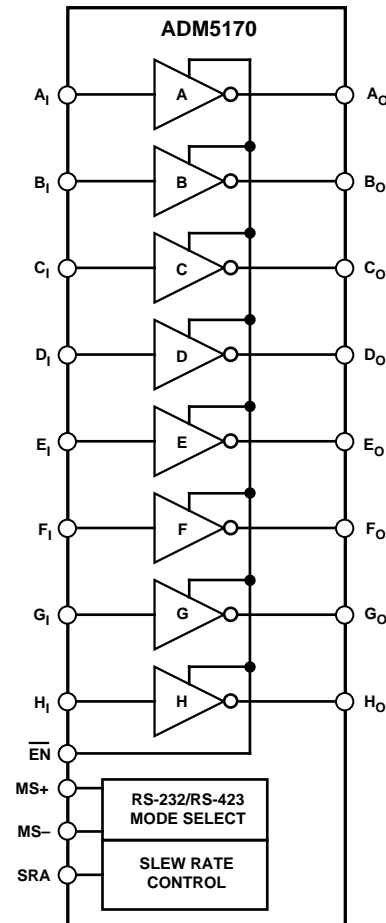
The ADM5170 is an octal line driver suitable for digital communication systems with data rates up to 116 kB/s. Input TTL or CMOS signal levels are inverted and translated into either EIA RS-232E or RS-423A signal levels depending on the status of the Mode Select inputs MS+ and MS-. With both Mode Select inputs at GND, RS-423 operation is selected while with MS+ connected to V_{DD} and MS- connected to V_{SS} , RS-232 operation is selected.

The output slew rates may be controlled using an external resistor connected between the SRA (Slew Rate Adjust) pin and GND. Resistor values between 2 k Ω and 10 k Ω may be selected giving a slew rate which can be adjusted from 10 V/ μ s to 2.2 V/ μ s. This adjustment of the slew rate allows tailoring of the output characteristics to suit the interface cable being used.

The outputs may be disabled using the \overline{EN} (Enable Input). This feature permits sharing of a common output line.

The ADM5170 is fabricated on an advanced CMOS process featuring low power consumption. In the disabled state the power consumption reduces from 500 mW to 40 mW. The ADM5170 is available in both 28-pin DIP and 28-lead PLCC packages.

FUNCTIONAL BLOCK DIAGRAM



Truth Table

Inputs		Outputs	
\overline{EN}	Data	EIA RS-232E ¹	RS-423A
0	0	($V_{DD} - 3$ V)	5 V to 6 V
0	1	($V_{SS} - 3$ V)	-5 V to -6 V
1	X	High Z	High Z

¹Minimum Output Level

REV. 0

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ADM5170* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADM5170: Octal, RS-232/RS-423 Line Driver Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADI RS-485/RS-422 Cross Reference Guide
- RS-232 Transceivers Cross Reference Guide

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- RS-232 Transceivers Applications Bulletin (Summer 2008)

Technical Articles

- Interface Primer

DESIGN RESOURCES

- ADM5170 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADM5170 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

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ADM5170—SPECIFICATIONS ($V_{DD} = +10\text{ V} \pm 10\%$, $V_{SS} = -10\text{ V} \pm 10\%$, $MS+ = MS- = 0\text{ V}$, $R_{SRA} = 10\text{ k}\Omega$. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD} Range	9		15	V	
V_{SS} Range	-9		-15	V	
I_{DD} (Disabled)		2	4	mA	$\overline{EN} = \text{High}$,
I_{DD} (Enabled)		25	36	mA	$R_L = \infty$, $\overline{EN} = 0\text{ V}$
I_{SS} (Disabled)		-2	-4	mA	$\overline{EN} = \text{High}$
I_{SS} (Enabled)		-23	-36	mA	$R_L = \infty$, $\overline{EN} = 0\text{ V}$
DIGITAL INPUTS					
Input Logic Threshold High, V_{INH}	2.0			V	
Input Logic Threshold Low, V_{INL}			0.8	V	
Input Clamp Voltage, V_{INK}		-1.1	-1.8	V	$I_{IN} = -15\text{ mA}$
Input High Level Current, I_{INH}			1	μA	$V_{INH} = 2.4\text{ V}$
Input Low Level Current, I_{INL}	-1			μA	$V_{INL} = 0.4\text{ V}$
OUTPUTS					
RS-423A Outputs					
High Level Output Voltage	5.0	5.3	6.0	V	$\overline{EN} = 0.8\text{ V}$, $MS+ = MS- = 0\text{ V}$ $R_L = \infty$, $V_{IN} = 0.8\text{ V}$
	5.0	5.3	6.0	V	$R_L = 3\text{ k}\Omega$, $V_{IN} = 0.8\text{ V}$
	4.5	5.2	6.0	V	$R_L = 450\ \Omega$, $V_{IN} = 0.8\text{ V}$
Low Level Output Voltage	-5.0	-5.3	-6.0	V	$R_L = \infty$, $V_{IN} = 2.0\text{ V}$
	-5.0	-5.6	-6.0	V	$R_L = 3\text{ k}\Omega$, $V_{IN} = 2.0\text{ V}$
	-4.5	-5.4	-6.0	V	$R_L = 450\ \Omega$, $V_{IN} = 2.0\text{ V}$
Output Balance, V_{BAL}		0.05	0.4	V	$R_L = 450\ \Omega$, $V_{BAL} = V_{OH} - V_{OL}$
RS-232 Outputs					
High Level Output Voltage	7.0	7.6	V_{DD}	V	$\overline{EN} = 0.8\text{ V}$, $MS+ = V_{DD}$, $MS- = V_{SS}$ $R_L = \infty$, $V_{IN} = 0.8\text{ V}$
	7.0	7.6	V_{DD}	V	$R_L = 3\text{ k}\Omega$, $V_{IN} = 0.8\text{ V}$
Low Level Output Voltage	-7.0	-7.7	V_{SS}	V	$R_L = \infty$, $V_{IN} = 2.0\text{ V}$
	-7.0	-7.7	V_{SS}	V	$R_L = 3\text{ k}\Omega$, $V_{IN} = 2.0\text{ V}$
Off-State Output Current, I_{OZ}	-100		100	μA	$\overline{EN} = 2.0\text{ V}$, $V_O = \pm 6\text{ V}$, $V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$
Short Circuit Current, I_{OS}	15	50	100	mA	$V_{IN} = 0\text{ V}$, $\overline{EN} = 0\text{ V}$
	15	40	100	mA	$V_{IN} = 5\text{ V}$, $\overline{EN} = 0\text{ V}$

Specifications subject to change without notice.

TIMING CHARACTERISTICS ($V_{DD} = +10\text{ V} \pm 10\%$, $V_{SS} = -10\text{ V} \pm 10\%$, $MS+ = MS- = 0\text{ V}$. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Slew Rate					Fig 1, Fig 2. $R_{SRA} = 2\text{ k}\Omega$, $R_L = 450\ \Omega$, $C_L = 50\text{ pF}$ Rising/Falling Edge, t_R , t_F
Output Slew Rate	6.65	10	14	V/ μs	
Output to Hi-Z Propagation Delay (Disable)		1.33	2.0	3	V/ μs Fig 1, Fig 2. $R_{SRA} = 10\text{ k}\Omega$, $R_L = 450\ \Omega$, $C_L = 50\text{ pF}$ Rising/Falling Edge, t_R , t_F
		0.3	1.0	μs	Fig 1, Fig 3. $R_{SRA} = 10\text{ k}\Omega$, $R_L = 450\ \Omega$, $C_L = 50\text{ pF}$ t_{HZ}
		0.5	1.0	μs	t_{LZ}
Hi-Z to Valid Output Propagation Delay (Enable)		6.0	15	μs	Fig 1, Fig 3. $R_{SRA} = 10\text{ k}\Omega$, $R_L = 450\ \Omega$, $C_L = 50\text{ pF}$ t_{ZH}
		7.0	15	μs	t_{ZL}

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD}	+15 V
V_{SS}	-15 V
Input Voltages	
V_{IN}	-0.3 to ($V_{DD} + 0.3$) V
Output Voltages	
V_{OUT}	-12 V to +12 V
Output Short Circuit Duration	Continuous
Power Dissipation Plastic DIP	1250 mW
(Derate at 12.5 mW/ $^\circ\text{C}$ above +50 $^\circ\text{C}$)	
θ_{JA} , Thermal Impedance	75 $^\circ\text{C}/\text{W}$
Power Dissipation PLCC	1000 mW
(Derate at 10 mW/ $^\circ\text{C}$ above +50 $^\circ\text{C}$)	
θ_{JA} , Thermal Impedance	80 $^\circ\text{C}/\text{W}$
Operating Temperature Range	
Commercial (J Version)	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$
Industrial (A Version)	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
Lead Temperature (Soldering 10 sec)	+300 $^\circ\text{C}$
Vapour Phase (60 sec)	+215 $^\circ\text{C}$
Infrared (15 sec)	+220 $^\circ\text{C}$

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM5170JN	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$	N-28
ADM5170AN	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	N-28
ADM5170JP	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$	P-28A
ADM5170AP	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	P-28A

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM5170 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

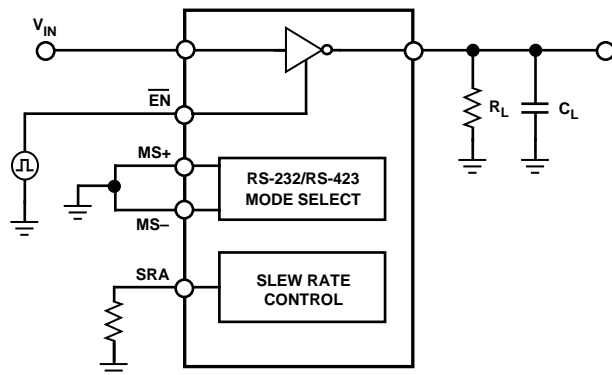


Figure 1. Timing Test Circuit

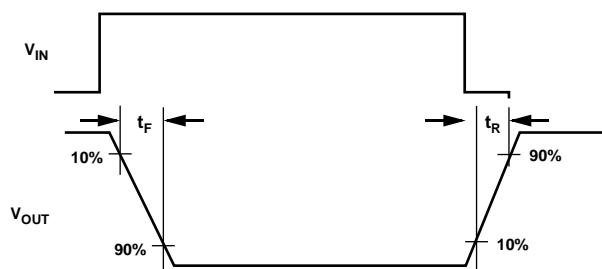


Figure 2. Rise/Fall Timing Waveforms

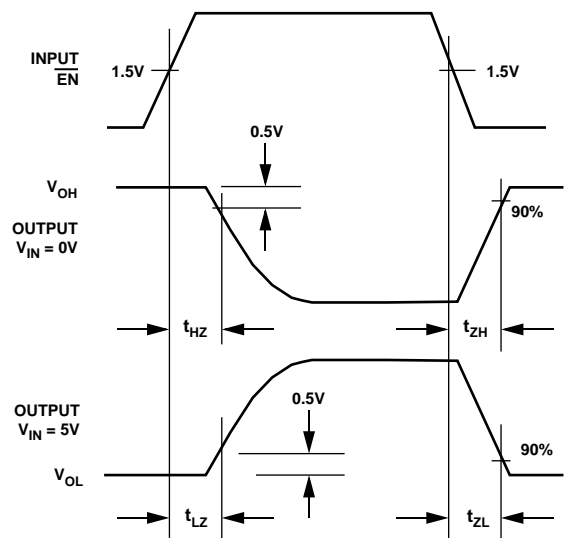
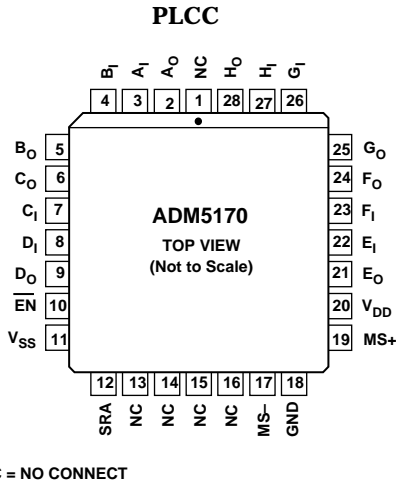
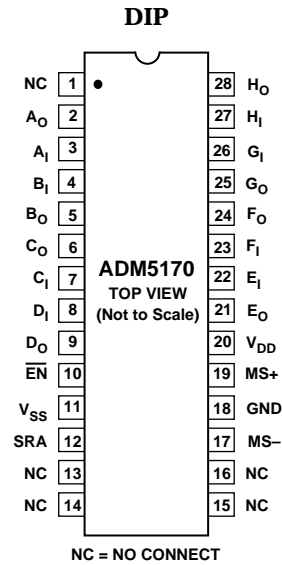


Figure 3. Enable/Disable Timing Waveforms

ADM5170

PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTION

Mnemonic	Function
V _{DD}	Power Supply Input, +10 V ± 10%.
V _{SS}	Power Supply Input, -10 V ± 10%.
GND	Ground Pin. Must be connected to 0 V.
A ₁ . . . H ₁	Digital Input to Drivers A to H.
A ₀ . . . H ₀	RS-232/RS-423 Output from Drivers A to H.
EN	Enable Pin. When high, all outputs are 3-stated.
MS+, MS-	Mode Select Inputs. Used to control the output level swing. With MS+ & MS- connected to GND, RS-423A output levels are selected. With MS+ connected to V _{DD} and MS- connected to V _{SS} , RS-232 output levels are developed.
SRA	Slew Rate Adjust Input. An external resistor (2 kΩ to 10 kΩ) connected between this pin and GND is used to control the Output Slew Rate (10 V/μs to 2.2 V/μs).

Slew Rate Programming

The slew rate for the ADM5170 is controlled by a single resistor connected between the SRA pin and GND. The slew rate is approximately.

$$\text{Slew Rate (V/}\mu\text{s)} = 20/R_{\text{SRA}} \text{ (k}\Omega\text{)}$$

Resistors between 2 kΩ and 10 kΩ may be used providing a slew rate which may be varied from 10 V/μs to 2.2 V/μs. Figure 5 in the Typical Performance Characteristics section shows how the slew rate varies with R_{SRA} while Figure 8 shows how the transition time (10% to 90%) varies with R_{SRA}. Waveshaping of the output allows the user to control the level of interference (near-end crosstalk) which may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rate are given in the EIA RS-423A specifications.

Maximum Data Rate (kB/s) = 300/t (for rates from 1 kB/s to 100 kB/s).

$$\text{Cable Length (feet)} = 100 \times t \text{ (Max Length = 4000 ft.)}$$

where *t* is the transition time (in μs) for the output to swing from 10% to 90% of its steady state values. The absolute maximum data rate is 100 kB/s and the maximum cable length is limited to 4000 ft.

Output Mode Programming

The ADM5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS-423A while the high output mode meets the RS-232 specifications. The high output mode provides greater output swings and is suitable for driving lines where higher attenuation levels must be tolerated. This mode is selected by connecting the mode select pins to the supplies, MS+ to V_{DD} and MS- to V_{SS}. The low output mode is selected by connecting both mode select pins MS+ and MS- to GND. This mode provides a controlled output swing with lower output levels.

Inputs				Outputs
MS+	MS-	EN	Data	Output
GND	GND	0	0	5 V to 6 V (RS-423)
GND	GND	0	1	-5 V to -6 V (RS-423)
V _{DD}	V _{SS}	0	0	(V _{DD} - 3 V) (RS-232) ¹
V _{DD}	V _{SS}	0	1	(V _{SS} + 3 V) (RS-232) ¹
X	X	1	X	High Z

¹Minimum Output Level.

Typical Application Circuit

A typical application circuit using a single driver in the ADM5170 is shown in Figure 4. This circuit is suitable for either RS-232 or RS-423 communication. An ADM5180 octal receiver is used to translate the signal back to CMOS logic level at the receiving end.

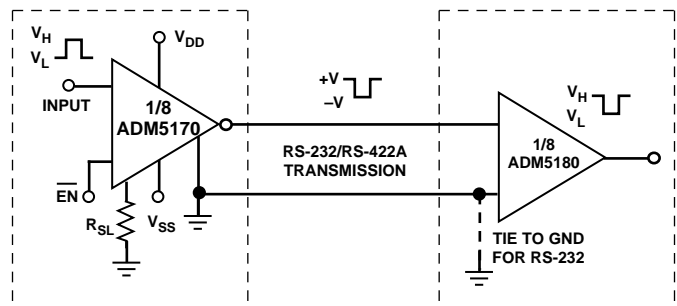


Figure 4. RS-232/RS-423A Typical Application Circuit

Typical Performance Characteristics–ADM5170

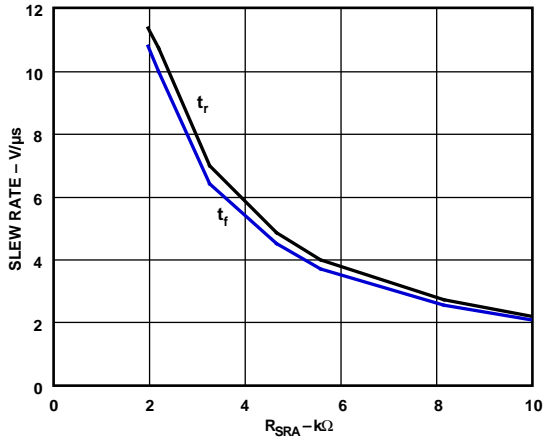


Figure 5. Typical Slew Rate vs. R_{SRA}

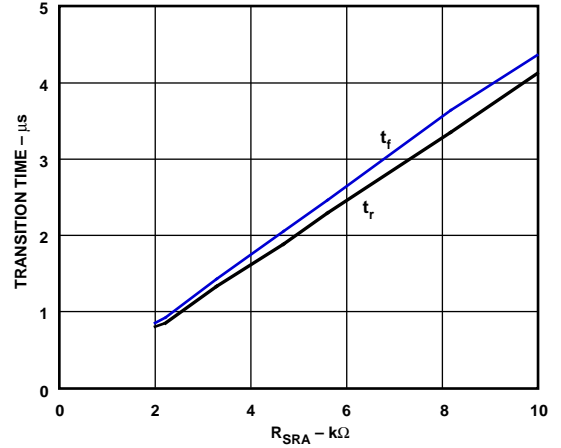


Figure 8. Typical Rise/Fall Times (RS-423A Mode) vs. R_{SRA}

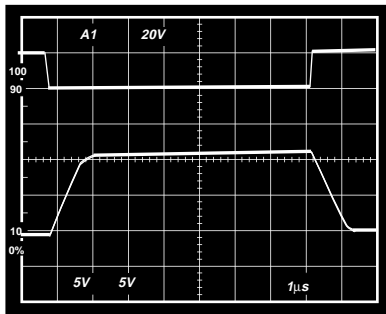


Figure 6. Slew Rate ($R_{SRA} = 2 \text{ k}\Omega$)

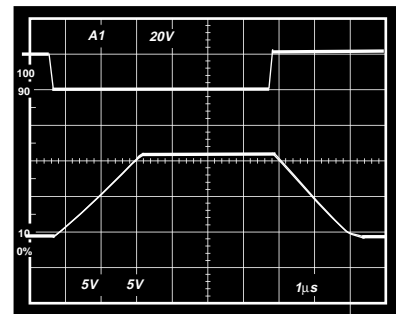


Figure 9. Slew Rate ($R_{SRA} = 10 \text{ k}\Omega$)

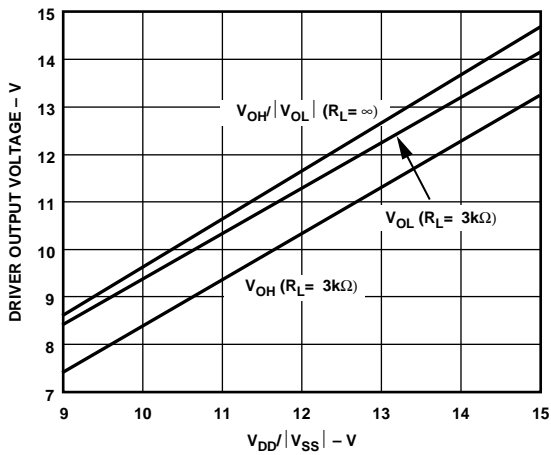


Figure 7. V_{OH}/V_{OL} vs. V_{DD}/V_{SS} (RS-232 Mode)

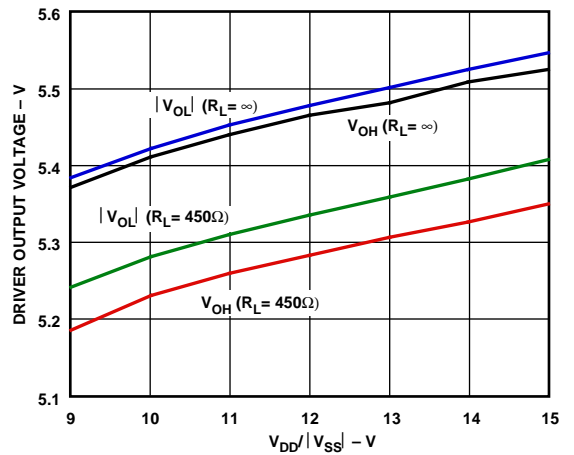


Figure 10. V_{OH}/V_{OL} vs. V_{DD}/V_{SS} (RS-423 Mode)

ADM5170

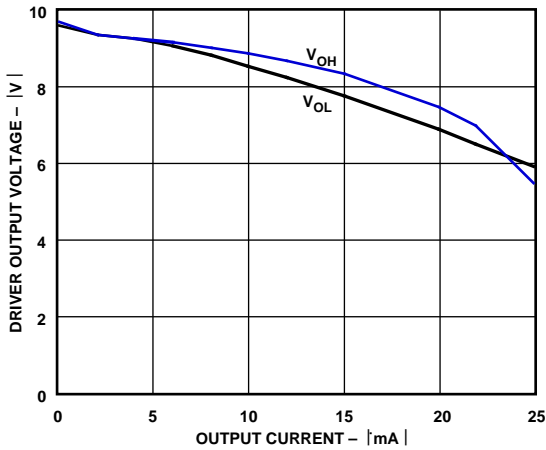


Figure 11. Driver Output Voltage vs. Output Current (RS-232 Mode)

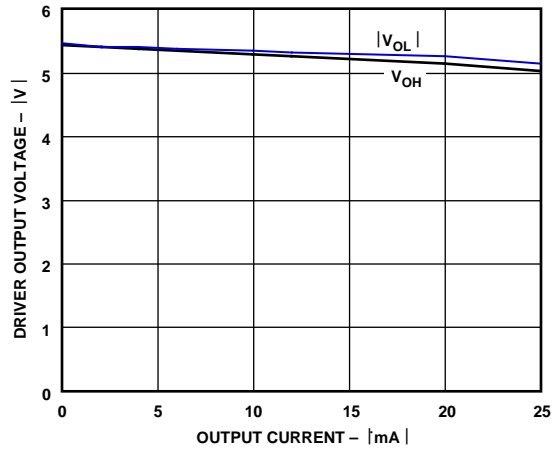
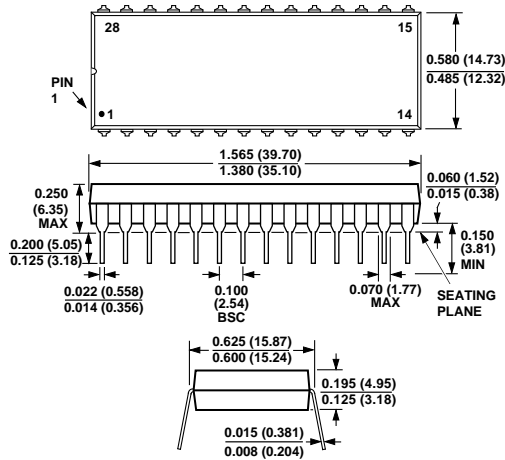


Figure 12. Driver Output Voltage vs. Output Current (RS-423 Mode)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Plastic DIP (N Suffix)



28-Lead Plastic Leaded Chip Carrier (PLCC) (P Suffix)

